I. Rejection of Claims 1-2, 6-8 and 10-12 under 35 U.S.C. §103

The Examiner has rejected Claims 1-2, 6-8 and 10-12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,251,740 B1 to Johnson, *et al.* ("Johnson"), or U.S. Patent No. 6,303,423 B1 to Lin ("Lin"), in view of U.S. Patent No. 6,025,226 to Gambino, *et al.* ("Gambino").

Johnson deals with the fabrication of a vertical plate capacitor in an interlayer dielectric material with conductors in upper and lower interconnect layers. (Abstract). The fabrication method in Johnson is directed to the avoidance of an accumulation of residual materials from chemical mechanical polishing to enable subsequent layers to be deposited thereon without contamination. (Col. 15, lines 49-53). Referring to the description of a dual damascene structure contained in the application, commencing on page 1, line 22, through page 2, line 4, Johnson does not describe such a structure. Johnson contains no teaching or suggestion regarding a method of forming a dual damascene structure.

Gambino does not overcome the shortcomings of Johnson. Gambino describes a method of manufacturing a capacitor simultaneously with the formation of the via portion of an interconnect structure, but does not teach or suggest a method of fabricating a capacitor together with a dual damascene structure. In contrast to the claimed inventions, Gambino describes a first interconnect layer formed upon a first interlevel dielectric, after which openings corresponding to vias and capacitors are extended through a second interlevel dielectric to the first interconnect layer, but grooves for interconnects are not formed. (Col. 7, lines 35-67, Col. 8, lines 1-53, FIGs.15-24). It should be specifically noted that all of the processes in Gambino are conducted without the use of etch stop layers as recited in the presently claimed inventions. There is simply no teaching or

suggestion in Gambino of forming a dual damascene structure and a capacitor in the way recited in the presently claimed inventions.

Lin addresses a process for creating high quality electrical components, such as inductors, capacitors or resistors, on a layer of passivation or on the surface of a thick layer of polymer. Lin also describes a process that provides a method of mounting discrete electrical components at a significant distance from the underlying silicon surface. Lin does not describe, teach, or suggest dual damascene structure, much less the formation of openings extending through a layer for a capacitor and a dual damascene structure. For the reasons noted above, Gambino does not overcome the shortcomings of Lin.

Because Johnson and Lin, in individual combination with Gambino, fail to teach or suggest the invention recited in independent Claims 1 and 10 and their dependent claims, when considered as a whole, the asserted combinations fail to establish a prima facie case of obviousness regarding Claims 1-2, 6-8 and 10-12. Because the cited references do not support the Examiner's rejection of Claims 1-2, 6-8 and 10-12 under 35 U.S.C. §103(a), the Applicant respectfully requests the Examiner to withdraw the rejection.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-2, 6-8 and 10-12.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.

Charles W. Gaines
Registration No. 36,804

Dated: 7/29/02

Hitt Gaines & Boisbrun, P.C.
P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) A method for manufacturing an integrated circuit comprising:

forming a layer having a stop layer;

[(a)] forming an opening [in a layer] for a dual damascene structure in the layer that includes at least a groove and a via where the via extends through the stop layer; and

[(b)] forming at least two openings in the layer for a capacitor having a first electrode and a second electrode, wherein the first and second electrodes are each defined by an opening that extends through the stop layer and the layer.

(2) Please amend Claim 2 as follows:

2. (Amended) The method of claim 1 wherein [steps (a) and (b)] forming an opening for a dual damascene structure and forming at least two openings in the layer for a capacitor occur at substantially the same time.

(3) Please cancel Claims 3-5 without prejudice or disclaimer.

(4) Please amend Claim 6 as follows:

6. (Amended) The method of claim 1 further comprising:

[(c)] filling the opening for a dual damascene structure with a conductive material [to form a dual damascene structure]; and

[(d)] filling the at least two openings in the layer for a capacitor with a conductive material [to form the capacitor].

(5) Please amend Claim 7 as follows:

7. (Amended) The method of claim 6 wherein [steps (c) and (d)] filling the opening for a dual damascene structure and filling the at least two openings in the layer for a capacitor occur at substantially the same time.

(6) Please cancel Claim 9 without prejudice or disclaimer.

(7) Please amend Claim 10 as follows:

10. (Amended) A method of manufacturing an integrated circuit comprising:

[(a)] forming a plurality of layers;

[(b)] partially forming a dual damascene structure by forming a first opening in a least one of the plurality of layers; and

[(c)] partially forming a capacitor by forming second and third openings in the at least one of the plurality of layers, wherein the second and third openings extend through the at least one of the plurality of layers.